Ordering number : ENN*6750

CMOS IC

LC86E6560

8-Bit Single Chip Microcontroller with the UVEPROM

Preliminary

Overview

The LC86E6560 is a CMOS 8-bit single chip microcontroller with UVERPOM for the LC866500 series. This microcontroller has the function and the pin description of the LC866500 series mask ROM version, and 60K-byte EPROM. The program data is rewritable. It is suitable to develop the program.

Features

(1) Option switching by EPROM data

The option function of the LC866500 series can be specified by the EPROM data.

LC86E6560 can be checked the functions of the trial pieces using the mass production board.

(2) Internal EPROM capacity : 61696 bytes

(3) Internal RAM capacity : 1152 bytes

Used EPROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86E6560.

Mask ROM version	EPROM capacity	RAM capacity
LC866560	61440 bytes	1152 bytes
LC866556	57344 bytes	1152 bytes

(4) Operating supply voltage : 4.5V to 6.0V

(5) Instruction cycle time : 1.0µs to 366µs

(6) Operating temperature : +10°C to +40°C

(7) The pin compatible with the LC866500 series mask ROM devices

(8) Applicable mask ROM version : LC866560/LC866556

(9) Factory shipment : QFC100S (with window)

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Notice for use

LC86E6560 is provided for the first release and small shipping of the LC866500 series.
At using, take notice of the followings.

(1) A point of difference LC86E6560 and LC866500 series.

Item	LC86E6560	LC866560/56
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by degrees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Pull-down resistor of the following pins • S0/T0 - S6/T6 • S7/T7 - S15/T15 • S16 -S31 • S32 - S47 • S48 -S51	Pull-down resistor provided/not provided Not provided Provided (fixed) Provided (fixed) Not provided Not provided	Pull-down resistor provided/not provided Specified by the option Provided (fixed) Specified by the option Specified by the option Not provided
Operating temperature range (Topg)	10°C to 40°C	-30°C to 70°C
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

LC86E6560 uses 256 bytes that is addressed on FF00H to FFFFH in the program memory as the option configuration data area. This option configuration cannot execute all options which LC866500 series have. Next tables show the options that correspond and not correspond to LC86E6560.

• A kind of the option corresponding of the LC86E6560

A kind of option	Pins, Circuits	Contents of the option
Input/output form of input/output ports	Port 0	1. N-channel open drain output 2. CMOS output *1
		1. Pull-up MOS Tr. provided 2. Pull-up MOS Tr. not provided *2
	Port 1 *1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output :CMOS
	Port 3 *1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output :CMOS

*1) Specified in a bit
*2) Specified in nibble unit. The port of N-channel open drain output does not have the Pull-up MOS Tr..

• A kind of the option not corresponding of the LC86E6560

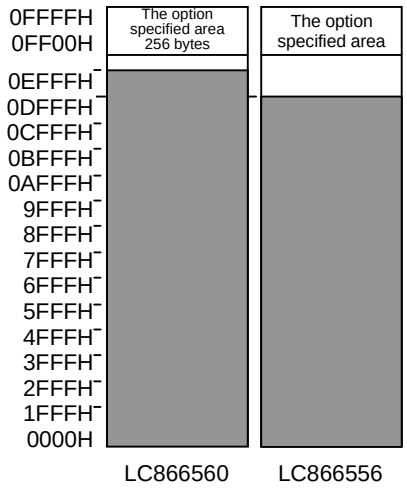
A kind of option	Pins, Circuits	LC86E6560	LC866560/56
Pull-down resistor of the high voltage withstand output terminals	• S0/T0 to S6/T6 • S16 to S31 • S32 to S47	Not provided Provided (fixed) Not provided	Specified by the option Specified by the option Specified by the option

(2) Option

The option data is created by the option specified program "SU86K.EXE". The created option data is linked to the program area by linkage loader "L86K.EXE".

(3) ROM space

LC86E6560 and LC866500 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 61440 bytes that is addressed on 0000H to EFFFH.


0FFFFH
0FF00H
0EFFFH
0DFFFH
0CFFFH
0BFFFH
0AFFFH
9FFFH
8FFFH
7FFFH
6FFFH
5FFFH
4FFFH
3FFFH
2FFFH
1FFFH
0000H
The option specified area 256 bytes
The option specified area
LC866560
LC866556

How to use

(1) Preparation

A complete evaluation (EVA) file must be converted to an INTEL-HEX formatted (HEX) file for program to the LC86E6560.

An EVA2HEX.EXE. can convert a EVA file to a HEX file.

Program the file that converted by the EVA2HEX to the LC86E6560.

(2) How to program for the EPROM

LC86E6560 can be programmed by the EPROM programmer with attachment ; W86EP6548Q.

• Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

• ”27512 (Vpp=12.5V) Intel high speed programming” mode available. The address must be set to “0 to 0FFFFH” and a jumper (DASEC) must be set to ‘OFF’ at programming.

(3) How to use the data security function

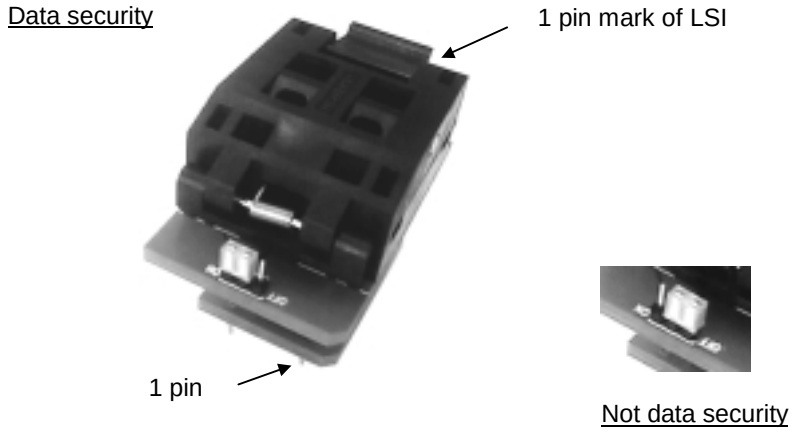
“Data security” is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

1. Set ‘ON’ the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have ‘FFH’ at the sequence 2 above.
- The programming by a sequential operation “BLANK⇒PROGRAM⇒VERIFY” cannot be executed data security at the sequence 2 above.
- Set to ‘OFF’ the jumper after executing the data security.



W86EP6548Q

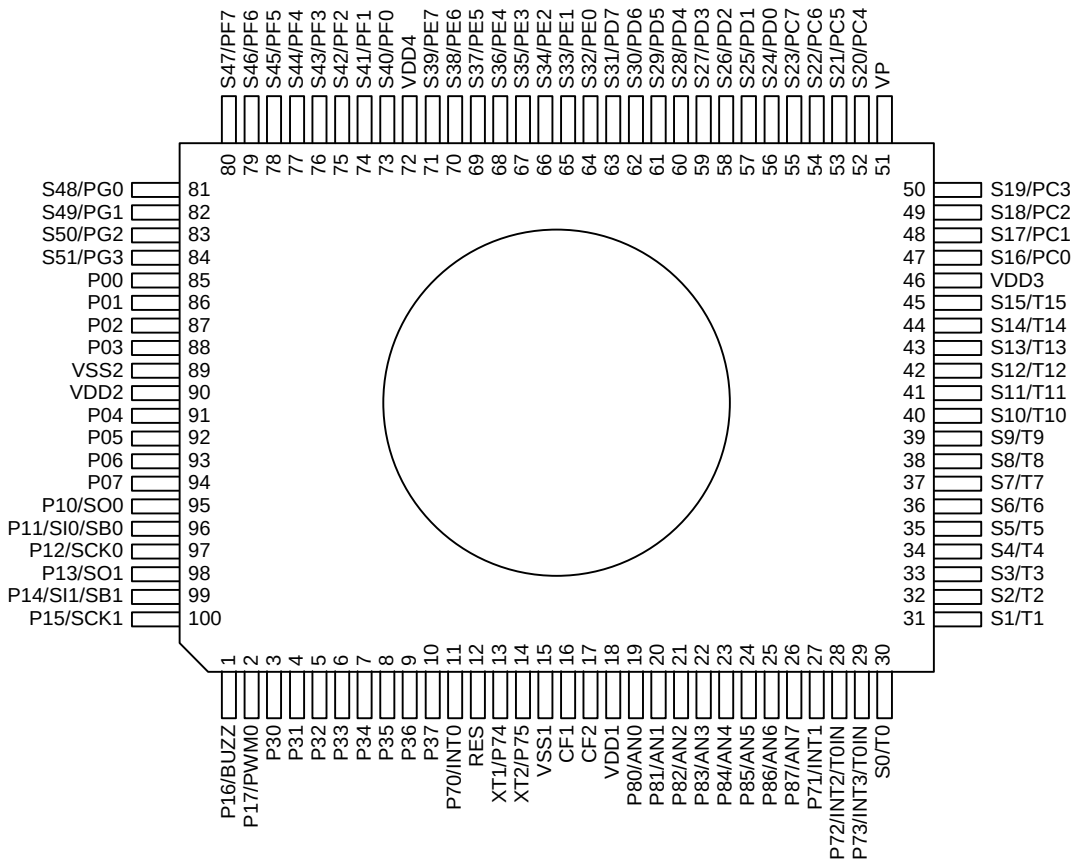
(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

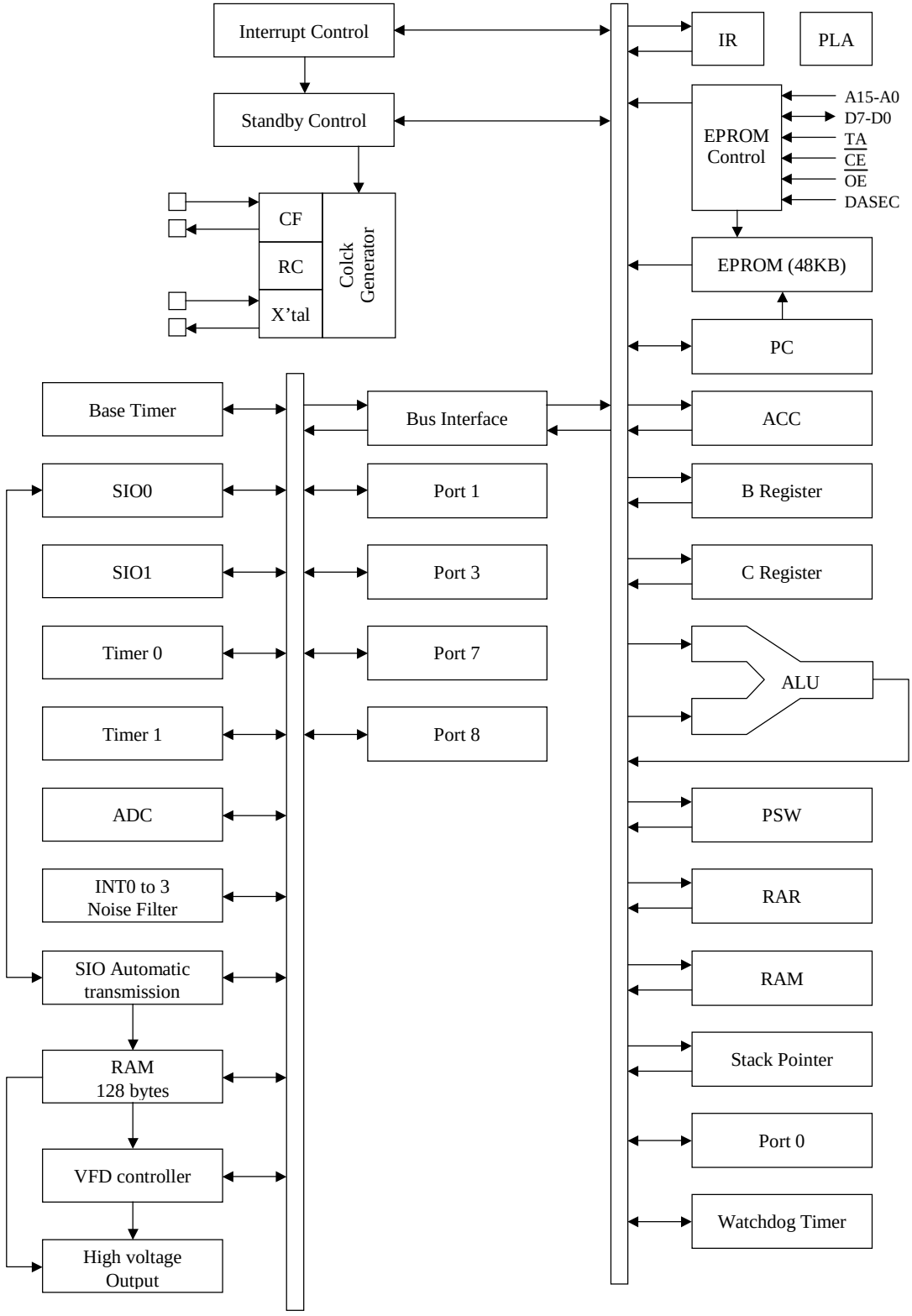
The UVEPROM (ultraviolet erasable programmable ROM) is in it. Put the seal on the window in use.

Pin Assignment



SANYO : QFC100S

System Block Diagram



Pin Description

Pin Name	I/O	Function description	Option	EPROM mode
VSS1, 2	-	Power pin (-) *4	-	-
VDD1, 2, 3, 4	-	Power pin (+) *4	-	-
VP	-	Power pin (+) for the VFD output pull-down resist	-	-
PORT 0 P00 - P07	I/O	•8-bit input/output port Input/output in nibble units •Input for port0 interrupt •Input for HOLD release •15V withstand at N-channel open drain output	•Pull-up resistor : Provided/not provided (each nibble) •Output form : CMOS/N-channel open drain (each bit)	-
PORT 1 P10 - P17	I/O	•8-bit input/output port Input/output can be specified in bit unit. •Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer1 output (PWM0 output)	Output form : CMOS/N-channel open drain (each bit)	Data line D0 to D7
PORT 3 P30 - P37	I/O	•8-bit input/output port Input/output in bit unit •15V withstand at N-channel open drain output	Output form : CMOS/N-channel open drain (each bit)	-
PORT 7 P70 - P73 $\overline{P74}$ - P75	 I/O I	•4-bit input/output port Input/output in bit unit •2-bit input port •Other pin functions P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer P71 : INT1 input/HOLD release input P72 : INT2 input/timer0 event input P73 : INT3 input with noise filter/timer0 event input $\overline{P74}$: 32.768kHz crystal oscillation terminal XT1 P75 : 32.768kHz crystal oscillation terminal XT2 •Interrupt received form, vector address	-	EPROM control signal DASEC(*1) $\overline{OE}$ (*2) $\overline{CE}$ (*3)
PORT 8 P80 -P83 P84 -P87	 I I/O	•4-bit input/output port Input/output in bit unit •4-bit input port •Other function AD input port (8 port pins)	-	-
S0/T0 to S6/T6 *6	O	Output for VFD display controller segment/timing in common	-	-
S7/T7 to S15/T15 *7	O	•Output for VFD display controller segment /timing with internal pull-down resistor in common •Internal pull-down resistor output	-	TA (*5)

	rising	falling	rising/ falling	H level	L level	Vector
INT0	enable	enable	disable	enable	enable	03H
INT1	enable	enable	disable	enable	enable	0BH
INT2	enable	enable	enable	disable	disable	13H
INT3	enable	enable	enable	disable	disable	1BH

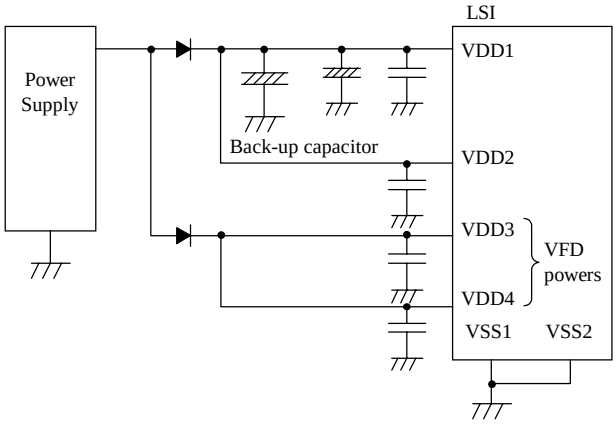
(Continue)

Pin Name	I/O	Function description	Option	EPROM mode
S16 to S31 *8	I/O	•Output for VFD display controller segment •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	-	Address input A15 to A0
S32 to S47 *9	I/O	•Output for VFD display controller segment •Other function S32 : High voltage input port PE0 S33 : High voltage input port PE1 S34 : High voltage input port PE2 S35 : High voltage input port PE3 S36 : High voltage input port PE4 S37 : High voltage input port PE5 S38 : High voltage input port PE6 S39 : High voltage input port PE7 S40 : High voltage input/output port PF0 S41 : High voltage input/output port PF1 S42 : High voltage input/output port PF2 S43 : High voltage input/output port PF3 S44 : High voltage input/output port PF4 S45 : High voltage input/output port PF5 S46 : High voltage input/output port PF6 S47 : High voltage input/output port PF7	-	-
S48 to S51 *9	I/O	•Output for VFD display controller segment •Other function S48 : High voltage input/output port PG0 S49 : High voltage input/output port PG1 S50 : High voltage input/output port PG2 S51 : High voltage input/output port PG3	-	-
$\overline{RES}$	I	Reset pin	-	-
XT1/ $\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation •Other function XT1 : Input port $\overline{P74}$ In case of non use, connect to VDD1.	-	-
XT2/P75	O	•Output pin for 32.768kHz crystal oscillation •Other function XT2 : Input port P75 In case of non use, connect to VDD1 at using as port or unconnect at using as oscillation.	-	-
CF1	I	Input pin for ceramic resonator oscillation	-	-
CF2	O	Output pin for ceramic resonator oscillation	-	-

* All of port options (except pull-up resistor of port 0) can be specified in bit unit.

(Continue)

*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 Connect like the following figure to reduce noise into a VDD1 terminal. Shorted the VSS1 terminal to the VSS2 terminal and to make the back-up time long.
*5 TA→EPROM control signal input
*6 S0/T0 to S6/T6 : not provided the pull-down resistor
*7 S7/T7 to S15/T155 : provided the pull-down resistor (fixed)
*8 S16 to S31 : provided the pull-down resistor (fixed)
*9 S32 to S51 : not provided the pull-down resistor



1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD1, VDD2 VDD3, VDD4	VDD1=VDD2 =VDD3=VDD4		-0.3		7.0	V
Input voltage		VI(1)	•Ports P74 , 75 •Ports 80, 81, 82, 83 •Port 8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-4.5		VDD+0.3	
Output voltage		VO	S0/T0 to S15/T15			VDD-4.5		VDD+0.3	
Input/output voltage		VIO(1)	•Port 1 •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87 •Ports 0, 3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
		VIO(3)	S16 to S51			VDD-4.5		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •For each pin.		-10			mA
		IOPH(2)	S0/T0 to S15/T15	At each pin.		-30			
		IOPH(3)	S16 to S51	At each pin.		-15			
	Total output current	∑IOAH(1)	Port 0	The total all pins.		-30			
		∑IOAH(2)	Ports 1, 3	The total all pins.		-30			
		∑IOAH(3)	S0/T0 to S15/T15	The total all pins.		-55			
		∑IOAH(4)	S16 to S27	The total all pins.		-60			
		∑IOAH(5)	S28 to S39	The total all pins.		-60			
		∑IOAH(6)	S40 to S51	The total all pins.		-60			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pin.				20	
		IOPL(2)	•Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87	At each pin.				15	
	Total output current	∑IOAL(1)	Port 0	The total all pins.				60	
		∑IOAL(2)	Ports 1, 3, 70	The total all pins.				50	
		∑IOAL(3)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	The total all pins.				20	
Maximum power dissipation		Pdmax	QFC100S	Ta=+10 to +40°C				500	mW
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				-55		+125	°C

2. Recommended Operating Range at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2=VDD3=VDD4	0.98μs≤tCYC≤400μs		4.5		6.0	V
Hold voltage	VHD	VDD1=VDD2	RAMs and registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	VP	VP		4.5 - 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 at CMOS output option	Output disable	4.5 - 6.0	0.33VDD+1.0		VDD	
	VIH(2)	Port 0 at N-ch open drain output	Output disable	4.5 - 6.0	0.75VDD		13.5	
	VIH(3)	•Port 1 •Ports 72, 73 •Port 3 at CMOS output option	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at N-ch open drain output	Output disable Tr. OFF	4.5 - 6.0	0.75VDD		13.5	
	VIH(5)	•Port 70 Port input /interrupt •Port 71 • $\overline{RES}$	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	4.5 - 6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports $\overline{P74}$, 75	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(8)	S16 to S51	Output P- channel Tr. OFF	4.5 - 6.0	0.33VDD+1.0		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	4.5 - 6.0	VSS		0.2VDD	V
	VIL(2)	Port 0 at N-ch open drain output	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1, 3 •Ports 72, 73	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 Port input /interrupt •Port 71 • $\overline{RES}$	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	4.5 - 6.0	VSS		0.8VDD-1.0	V
	VIL(6)	•Port 8 •Ports $\overline{P74}$, 75	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(7)	S16 to S51	Output P- channel Tr. OFF	4.5 - 6.0	VP		0.2VDD	
Operation cycle time	tCYC			4.5 - 6.0	0.98		400	μs

(Continue)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	6MHz (ceramic resonator oscillation) Refer to figure 1	4.5 - 6.0		6		MHz
	FmCF(2)	CF1, CF2	3MHz (ceramic resonator oscillation) Refer to figure 1	4.5 - 6.0		3		
	FmRC		RC oscillation	4.5 - 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	32.768kHz (X'tal oscillation) Refer to figure 2	4.5 - 6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	6MHz (ceramic resonator oscillation) Refer to figure 3	4.5 - 6.0				ms
	tmsCF(2)	CF1, CF2	3MHz (ceramic resonator oscillation) Refer to figure 3	4.5 - 6.0				
	tssXtal	XT1, XT2	32.768kHz (X'tal oscillation) Refer to figure 3	4.5 - 6.0				s

(Note 1) The oscillation constant is shown on table 1.

3. Electrical Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	Ports 0, 3 of open drain output	•Output disable •VIN=13.5V (including the off-leak current of the output Tr.)	4.5 - 6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1, 3	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including the off-leak current of the output Tr.)	4.5 - 6.0			1	
	IIH(3)	•Ports 70, 71, 72, 73 •Port 8	•Output disable •VIN=VDD (including the off-leak current of the output Tr.)	4.5 - 6.0			1	
	IIH(4)	$\overline{\text{RES}}$	VIN=VDD	4.5 - 6.0			1	
	IIH(5)	Ports $\overline{\text{P74}}$, 75	VIN=VDD	4.5 - 6.0			1	
	IIH(6)	S32 to S51 without pull-down resistor	•Output P-channel Tr. OFF •VIN=VDD	4.5 - 6.0			1	
Input low current	IIL(1)	•Ports 1, 3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.)	4.5 - 6.0	-1			
	IIL(2)	•Ports 70, 71, 72, 73 •Port 8	•Output disable •VIN=VSS (including the off-leak current of the output Tr.)	4.5 - 6.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	4.5 - 6.0	-1			
	IIL(4)	Ports $\overline{\text{P74}}$, 75	VIN=VSS	4.5 - 6.0	-1			
Output high voltage	VOH(1)	Ports 0, 1, 3 of CMOS output	IOH=-1.0mA	4.5 - 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5 - 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 - 6.0	VDD-1.8			
	VOH(4)		•IOH=-1mA •The current of any unmeasurement pin is not over 1 mA.	4.5 - 6.0	VDD-1			
	VOH(5)	S16 to S51	IOH=-5mA	4.5 - 6.0	VDD-1.8			
	VOH(6)		The current of any unmeasurement pin is not over 1mA.	4.5 - 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1, 3	IOL=10mA	4.5 - 6.0			1.5	V
	VOL(2)		IOL=1.6mA	4.5 - 6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5 - 6.0			0.4	
	VOL(4)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	IOL=1.6mA	4.5 - 6.0			0.4	
Pull-up MOS Tr. resistance	Rpu	Ports 0, 1, 3	VOH=0.9VDD	4.5 - 6.0	15	40	70	kΩ

(Continue)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output off-leakage current	IOFF(1)	S0/T0 to S6/T6, S32 to S51 without pull-down resistor	•Output P-ch Tr. OFF •VOUT=VSS	4.5 - 6.0	-1			μA
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5 - 6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S51	•Output P-ch Tr. OFF •Using as input ports	4.5 - 6.0		200		kΩ
High voltage pull-down resistor	Rpd	•S7/T7 to S15/T15 •S16 to S31	•Output P-ch Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	
VP pull-down resistor	Rvppd	Vp	•VSS=GND •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73, 75 • $\overline{\text{RES}}$	Output disable	4.5 - 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz Unmeasurement terminals for input are set to VSS level. •Ta=25°C	4.5 - 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCK1	Refer to figure 5.	4.5 - 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	4.5 - 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set up time		tICK	•SI0, SI1 •SB0, SB1	•Data set-up to SCK0, 1. •Data hold from SCK0, 1. •Refer to figure 5.	4.5 - 6.0	0.1			μs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1. •Refer to figure 5.	4.5 - 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock)		tCKO(2)			4.5 - 6.0			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5 - 6.0	200			μs

6. AD Converter Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N			4.5 - 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 - 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time =16×tCYC (ADCR2=0) (Note 3)	4.5 - 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time =32×tCYC (ADCR2=1) (Note 3)	4.5 - 6.0	31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5 - 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 6.0			1	μA
	IAINL		VAIN=VSS	4.5 - 6.0	-1			

(Note 2) Absolute precision does not include quantizing error (±1/2LSB).
(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=+10°C to +40°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •Internal RC oscillation stops •FmX'tal=32.768kHz X'tal oscillation •System clock : CF oscillation •1/1 divided	4.5 - 6.0		14	33	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •Internal RC oscillation stops •FmX'tal=32.768kHz X'tal oscillation •System clock : CF oscillation •1/2 divided	4.5 - 6.0		6	18	
	IDDOP(3)		•FmCF=0Hz (When oscillation stops.) •FmX'tal=32.768kHz X'tal oscillation •System clock : RC oscillation •1/2 divided	4.5 - 6.0		4	13	
	IDDOP(4)		•FmCF=0Hz (When oscillation stops.) •FmX'tal=32.768kHz X'tal oscillation •System clock : X'tal oscillation •Internal RC oscillation stops. •1/2 divided	4.5 - 6.0		3	10	

(Continue)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •Internal RC oscillation stops •FmX'tal=32.768kHz X'tal oscillation •System clock : CF oscillation •1/1 divided	4.5 - 6.0		5	14	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •Internal RC oscillation stops •FmX'tal=32.768kHz X'tal oscillation •System clock : CF oscillation •1/2 divided	4.5 - 6.0		2.2	7	mA
	IDDHALT(3)		•HALT mode •FmCF=0Hz (When oscillation stops.) •FmX'tal=32.768kHz X'tal oscillation •System clock : RC oscillation •1/2 divided	4.5 - 6.0		400	1600	μA
	IDDHALT(4)		•HALT mode •FmCF=0Hz (When oscillation stops.) •FmX'tal=32.768kHz X'tal oscillation •System clock : X'tal oscillation •Internal RC oscillation stops. •1/2 divided	4.5 - 6.0		25	100	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)		HOLD mode	4.5 - 6.0		0.05	30	μA

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	TBD		
	Kyocera			
3MHz ceramic resonator oscillation	Murata			
	Kyocera			

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd	Rf
32.768kHz crytal oscillation						

* Both C3 and C4 must be a J rank (±5%) and CH characteristics.
(K rank (±10%), SL characteristics parts can be used for the applications which do not require oscillation accuracy.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

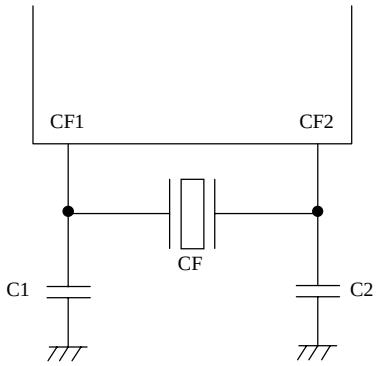


Figure 1 Ceramic oscillation circuit

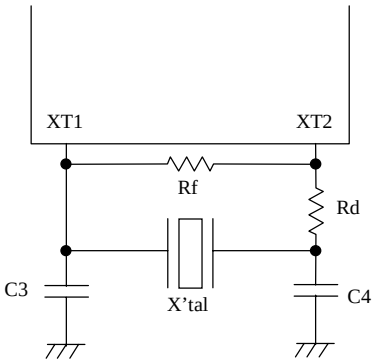


Figure 2 Crystal oscillation circuit

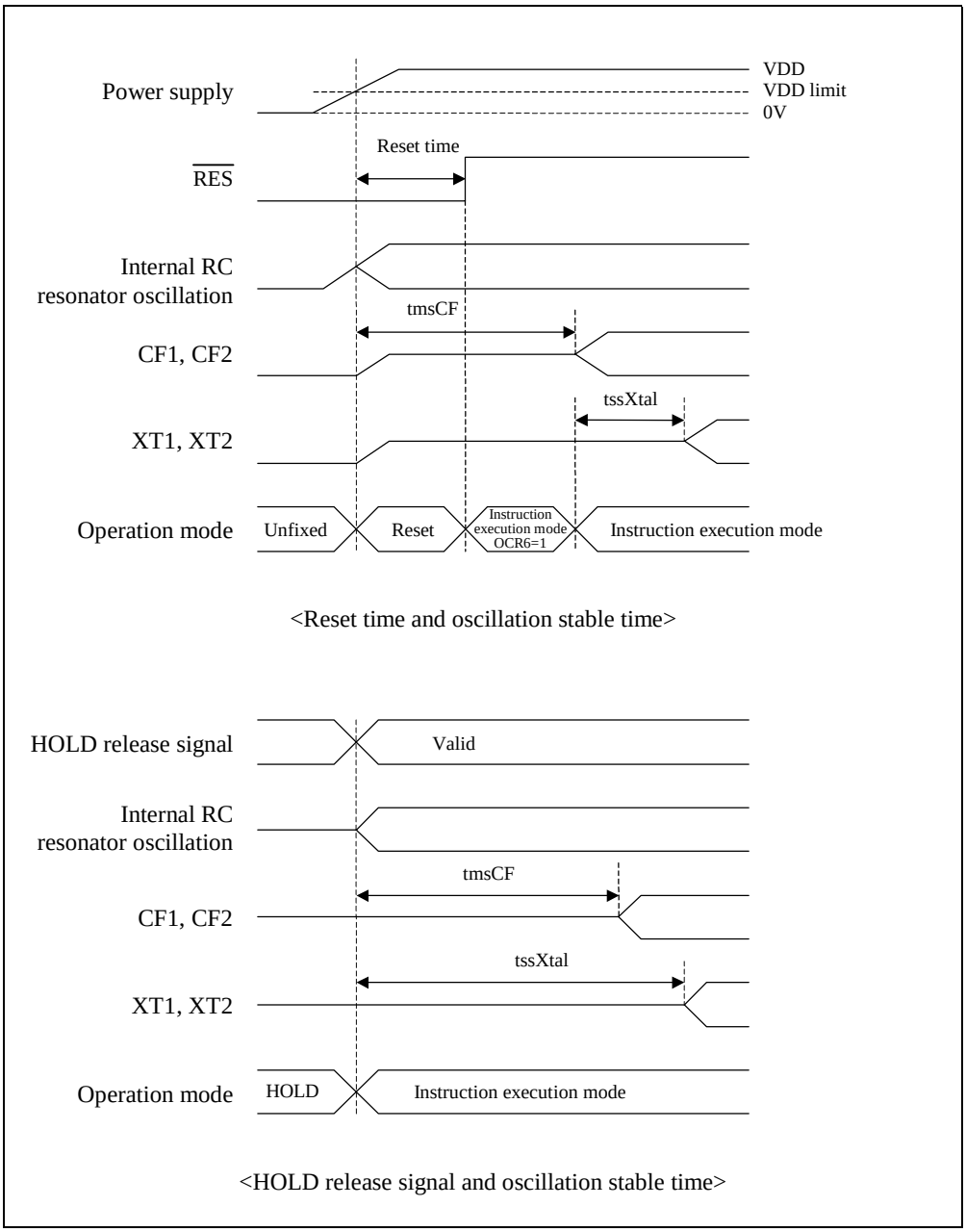
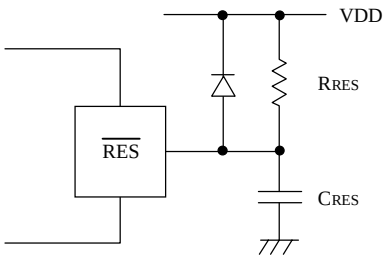


Figure 3 Oscillation stabilizing time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

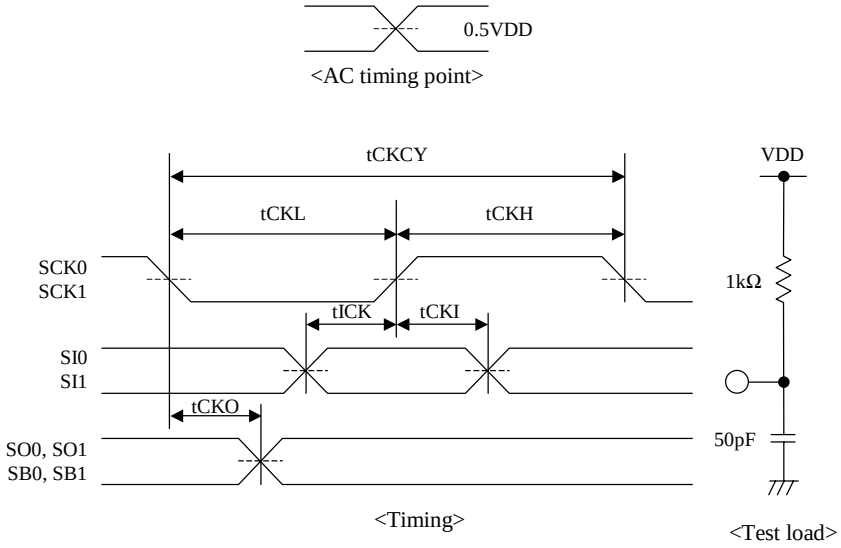


Figure 5 Serial input / output test condition

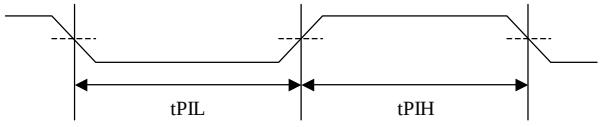


Figure 6 Pulse input timing condition